REMARKS/ARGUMENTS

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on April 19, 2006. This Response has been prepared pursuant to comments and suggestions made during the interview.

Claims 1-25 are pending in the present application. Claims 1, 3, 8, 9, 11, 12, 13, 16, 17, 19, 20, 23 and 24 are amended. No claims are added and no claims are canceled. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

A new, more descriptive title has been provided as required by the Examiner. In addition, the serial numbers of related applications referred to on pages 1 and 2 of the specification have been provided as requested by the Examiner.

The informalities noted by the Examiner in claims 9, 17 and 23; as well as informalities noted in claims 11, 20 and 24, have been corrected. The Examiner is thanked for bringing the informalities to Applicants' attention.

I. 35 U.S.C. § 101

The Examiner has rejected claims 19-25 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

Applicants believe claims 19-25 are directed to statutory subject matter. In order to expedite prosecution, however, the objectionable language in the specification has been deleted. Withdrawal of the rejection under 35 U.S.C. § 101 is, accordingly, respectfully requested.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-25 under 35 U.S.C. § 102(a) as being anticipated by Davidson et al. (U.S. Patent No. 6,574,727). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states as follows:

> As per claim 1, Davidson discloses a method in a data processing system for monitoring processing of instructions, the method comprising:
> receiving an instruction at a processor for execution; (Col. 8 lines 58-60)
> responsive to being in an enabled state, (Col. 11, lines 35-55) determining whether the instruction is associated with an indicator in a shadow memory; (Col. 8, line 65-col. 9 line 8) *The examiner asserts that the value to be matched must be stored in some sort of memory, as the value could not be retained if it wasn't.*

and performing a selected action in response to the indicator being associated with the instruction. (Col. 8 lines 30-36)

Office Action dated January 30, 2006, page 4.

Claim 1 as amended herein is as follows:

1. A method in a data processing system for monitoring processing of instructions, the method comprising:

receiving an instruction at a processor for execution;

responsive to a determination of being in an enabled state to perform a selected action, determining whether the instruction is associated with an indicator stored in a shadow memory, the shadow memory comprising a storage area separate from an instruction storage area in which the instruction is stored; and

performing the selected action in response to the indicator being associated with the instruction.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Davidson et al. (hereinafter "Davidson") does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to amended claim 1, in particular, Davidson does not teach or suggest "responsive to a determination of being in an enabled state to perform a selected action, determining whether the instruction is associated with an indicator stored in a shadow memory, the shadow memory comprising a storage area separate from an instruction storage area in which the instruction is stored".

Davidson is directed to a mechanism for selecting an instruction to be monitored within a pipelined processor. In particular, Davidson discloses that when instructions are fetched, they are matched against at least one match condition to generate instructions that are eligible for sampling. The instructions eligible for sampling are then sampled to generate sampled instructions, and the sampled instructions are marked in order that they may be monitored while executing within the pipelined processor. Col. 8, line 65-col. 9, line 8 referred to by the Examiner in rejecting the claims reads as follows:

Instruction match facility **604** may be used to identify instructions by their opcode and/or extended opcode by matching the fetched instructions against selected opcodes. The matching may be performed through the use of one or more mask registers. A matched instruction is signified through a bit in the pre-decode information that is stored with the instruction in the instruction cache. Match bit **606** and opcode/instruction bits **608** are then stored in instruction cache **610** until selection for progress through the remainder of the instruction pipeline.

Davidson, as described above, teaches that instructions are identified by their opcode and/or extended opcode by matching the fetched instructions against selected opcodes. Davidson does not disclose, either in the above recitation, or elsewhere in the patent, that an indicator with which an instruction is associated is stored "in a shadow memory that comprises a storage area separate from an instruction storage area in which the instruction is stored" as now recited in claim 1. Although the Examiner asserts that "the value to be matched must be stored in some sort of memory" in order to be retained, the reference does not disclose or suggest that a value to be matched is stored in a shadow memory that comprises "a storage area separate from an instruction storage area in which the instruction is stored" as required by claim 1. Claim 1, accordingly, is not anticipated by Davidson and patentably distinguishes over Davidson in its present form.

Claims 2-7 depend from and further restrict claim 1 and are also not anticipated by Davidson, at least by virtue of their dependency.

Independent claims 12 and 19 are system and computer program product claims that correspond to claim 1, and have been amended in a similar manner as claim 1. These claims, together with dependent claims 13-15 and 20-22 are not anticipated by Davidson for substantially the same reasons as discussed above with respect to claim 1, and also patentably distinguish over Davidson in their present form.

Independent claim 8, as amended herein is as follows:

8. A method in a data processing system for monitoring access to data during execution of instructions by a processor, the method comprising:

responsive to a determination of being in an enabled state to perform a selected action when a data access to a memory location occurs, determining whether the memory location is associated with an indicator stored in a shadow memory, the shadow memory comprising a storage area separate from the memory location in which data is stored; and

performing the selected action in response to the indicator being associated with the memory location.

For similar reasons as discussed above with respect to claim 1, Davidson does not disclose or suggest "responsive to a determination of being in an enabled state to perform a selected action when a data access to a memory location occurs, determining whether the memory location is associated with an

indicator stored in a shadow memory, the shadow memory comprising a storage area separate from the memory location in which data is stored". Davidson does not disclose a shadow memory, and does not disclose or suggest that an indicator with which a memory location is associated is stored in a shadow memory that is separate from a memory location in which data is stored. Claim 8, accordingly, is also not anticipated by Davidson and should be allowable in its present form, together with claims 9-11 dependent thereon.

Independent claims 16 and 23 are system and computer program product claims that correspond to claim 8 and are also not anticipated by Davidson for similar reasons as discussed above with respect to claim 8. Claims 17-18 and 24-25 depend from and further restrict claims 16 and 23 and are also not anticipated by Davidson, at least by virtue of their dependency.

Therefore, the rejection of claims 1-25 under 35 U.S.C. § 102 has been overcome.

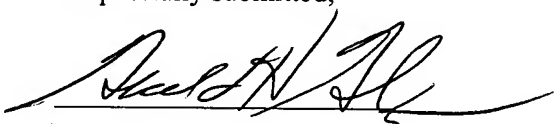
III. Conclusion

For all the above reasons, it is respectfully urged that claims 1-25 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: April 27, 2006

Respectfully submitted,



Gerald H. Glanzman
Reg. No. 25,035
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants